

Docket No.: R2184.0247/P247
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Keiichi Yoshioka

Application No.: Not Yet Assigned

Confirmation No.: @@@

Filed: Concurrently Herewith

Art Unit: N/A

For: SEMICONDUCTOR INTEGRATED
CIRCUIT DEVICE AND FABRICATION
METHOD THEREOF

Examiner: Not Yet Assigned

CLAIM FOR PRIORITY

MS Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant hereby claims priority under 35 U.S.C. 119 based on the following
prior foreign application filed in the following foreign country on the date indicated:

<u>Country</u>	<u>Application No.</u>	<u>Date</u>
Japan	2002-232551	August 9, 2002

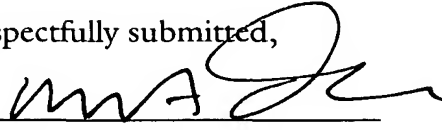
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In support of this claim, a certified copy of the said original foreign application will be filed shortly.

Dated: August 5, 2003

Respectfully submitted,

By 

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